- APROVIS3D -

Analog PROcessing of bioinspired VIsion Sensors for 3D reconstruction

Document Reference:		
Title: **D2.1.2 EF-DVS Integrated Prototype and Test**		
Contractor: **IMSE**		
Prepared by: **Teresa Serrano-Gotarredona**		
Document Type: **Deliverable**		
Version: **1**		Pages:
Classification: **External document**		

Document Track

Version	Date	Remarks and Authors
1.0	03/11/2022	First draft (T. Serrano - IMSE)
2.0		Final version ()

Authors

	Role / Function	Name	Organisation
Prepared by	WP2 Leader	T. Serrano-G.	IMSE
Checked by	Quality check		
Released by			
Approved by			

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1 Introduction

Among the collection of spiking vision sensors, the DVSs (dynamic vision sensors) due to their low pixel mismatch, high dynamic range, high pixel bandwidth, low latency, low power consumption and temporal redundancy data suppression properties have become very popular and have raised the industrial interest. Several spin-off companies (PROPHESEE [1], CELEPIXEL [2] or INIVATION [3,4]) have put in the market high-resolution prototypes and other established companies as Samsung [5] and Sony (https://www.sony.net/SonyInfo/News/Press/202002/20-0219E/), have also developed DVS prototypes. Megapixel DVSs allow performing high-resolution detection of small objects while keeping a broad field of view. However, the data rate produced by the sensor may saturate the sensor output bandwidth especially if the observed image has high dynamic contents as it is the case of fast car driving. Furthermore, as the sensor resolution increases, it also increases the size and energy consumption of the subsequent vision processing systems. Alternatives to improve the sensor bandwidth have been proposed as communicating in parallel the events of a group of pixels [5]. Other alternatives aim at reducing the amount of sensor output data by including a spatio-temporal correlation logic block shared by a group of pixels to filter out noisy pixels as well as reduce spatial redundancy [4] or by including a digital event signal processor at the sensor output that can be programmed with some spatio-temporal filtering capabilities [1]. These late alternatives [1,4] aim to increase the sparseness in the output data but the size complexity of the subsequent processing system remains the same. This dilemma is solved in some biological systems. Humans are equipped with *foveal vision* [6].
Our eyes have a foveal region equipped with a high density of color sensitive photodetectors where a high resolution (HR) vision is sensed. The photoreceptor density decreases logarithmically towards the peripheral region where color insensitive low resolution (LR) scene parts are acquired [7]. High-speed localization of objects of interest is performed using computation on peripheral low resolution regions (also known as the 'where' computation) to control the eye saccade movements that center the foveal fixation point on the target region that will be processed with high resolution for further observation and processing by the recognition 'what' subsystem. Not only are less the retina resources dedicated to acquire the peripheral regions, but also the cortical area of computational resources dedicated to process the peripheral regions are less. Whereas the foveal region corresponds to only 5º of the visual field, 25% of the cortical computational resources are dedicated to process it. **Figure 1**(a) illustrates the proposed electronically multi-foveated vision system. The top subfigure in **Figure 1**(a) illustrates a moderate resolution image with 259,2k pixels. The lower subfigure illustrates a x64 lower resolution representation with 4k pixels that would be used by the LR Deep-Net attention subsystem in **Figure 1**(b) to localize the ROIs (regions of interest) in the visual field and control electronically the foveation regions where a high resolution object recognition is done simultaneously in parallel over small regions by the HR recognition subsystems, reducing the computation demands that would be needed for processing the full image.

The use of foveated vision to achieve efficient object recognition of high-resolution target objects combined with a wide low resolution vision field allowing localizing the target in peripheral regions with low computational load has been previously proposed. In the robotic vision community, hardware systems combining several cameras with different vision fields have been proposed [8,9]. However, these systems require mechanical control to move the central point of the foveation sensor which increases the system delay and power consumption. Other systems are based on the use of high resolution sensors and a foveal transformation is done in subsequent processing stages to save computation power and energy. However, these systems do not alleviate the data bandwidth communication at the sensor level [10,11]. There have been some proposals of sensors with foveal physical geometry; many of them suffer from non-optimum use of the silicon area [12–14]. A sensor with uniform high resolution foveal pixels in the center and low resolution motion detection peripheral pixels has been

proposed [15], however it still needs a mechanical control of the center of foveation. A foveated sensor with electronic control of the foveation point where spatial resolution is traded off for temporal resolution has been published [16]. However, it does not reduce the output data rate of the sensor.

During **APROVIS3D**, IMSE has implemented a first prototype of an electronically foveated dynamic vision sensor EF-DVS. The foveation regions are configurable with external electronic signals. Multiple foveation points and region sizes can be electronically activated. An EF-DVS of resolution 128x128 has been implemented in AMS 0.35 micron technology. The sensor design has been reported in Deliverable D2.1.1. In the current deliverable we describe the sensor top level connectivity and control, the design of the test PCB, and and demonstrate its functionality with preliminary experimental results.

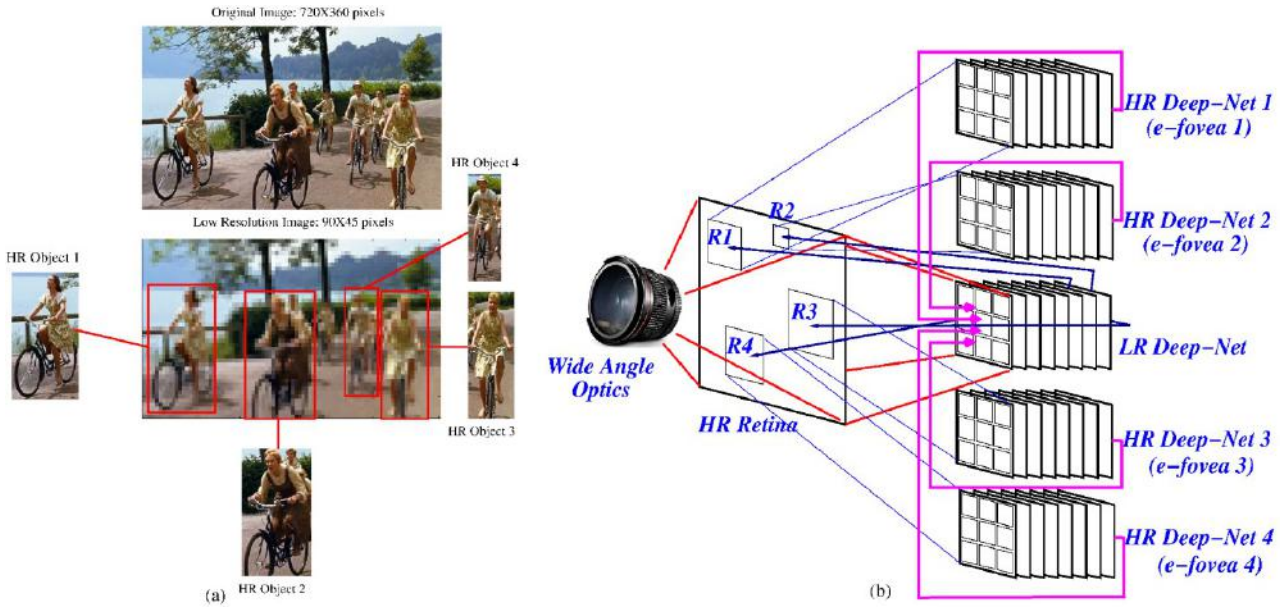
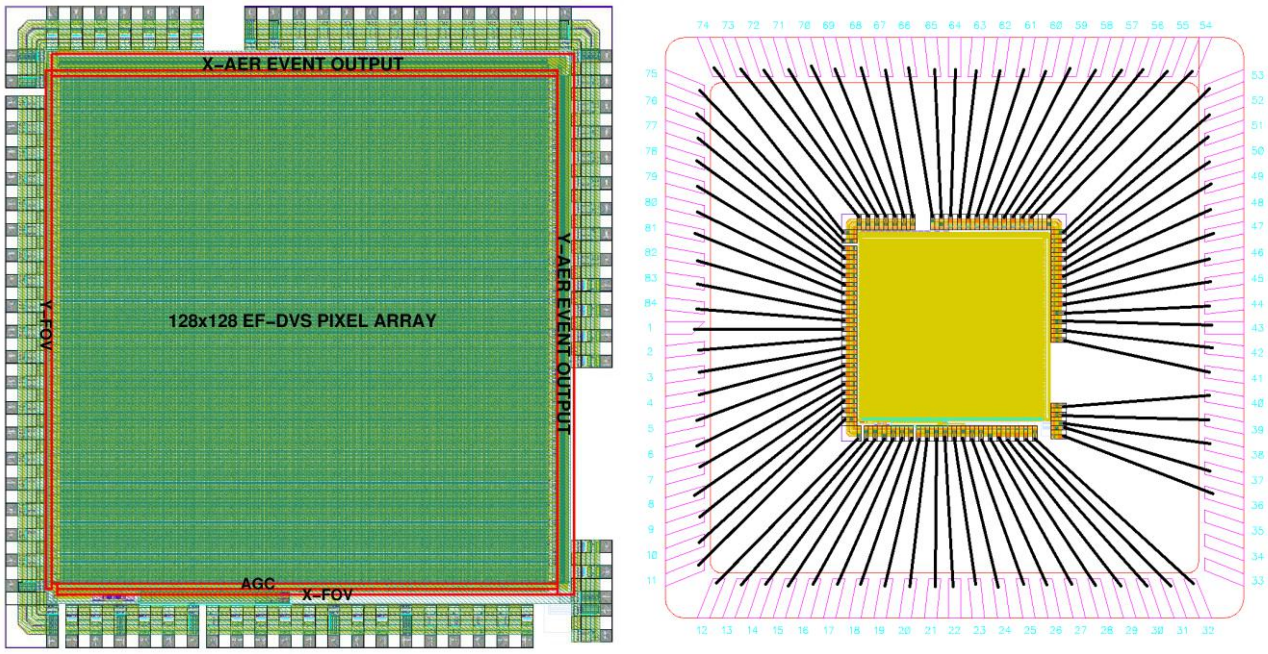


Figure 1. Illustration of a multifoveal resolution sensor, and (b) proposed vision system with electronic control of multiple foveation points and parallel object recognition subsystems.



(b)

Figure 2. EF-DVS sensor (a) layout in AMS-0.35 OPTO Technology (b) packaged in a JLCC84

2 Sensor Architecture, Biasing and Control

An EF-DVS implementing the first proposed foveated architecture has been designed in AMS 0.35 OPTO technology. The prototype contains an array of 128x128. **Figure 2**(a) plots the full layout of the EF-DVS sensor in the AMS 0.35 OPTO technology. The total chip area is 5,02x5,05 mm^2 including the pads. In **Figure 2**(a), the area dedicated to the main circuit blocks is indicated. The sensor is fully covered with a shielding of metal 4 except for the photodetector areas. The chip has been packaged in JLCC84 package. The bonding diagram of the chip is plotted in **Figure 2**(b). The table below contains a brief description of the pinout of the chip. The role of the different pins will be detailed in the next subsections.

Pin No	Schematic Name	Type	Description
1	fax<6>	I – digital input	Bit of x-word input address for foveal configuration
2	fax<5>	I – digital input	Bit of x-word input address for foveal configuration
3	fax<4>	I – digital input	Bit of x-word input address for foveal configuration
4	fax<3>	I – digital input	Bit of x-word input address for foveal configuration
5	fax<2>	I – digital input	Bit of x-word input address for foveal configuration
6	fax<1>	I – digital input	Bit of x-word input address for foveal configuration
7	fax<0>	I – digital input	Bit of x-word input address for foveal configuration
8	AEX	I – digital input	Enable all column selection in foveal config when high
9	mdX	I – digital input	Signal configuring horizontal foveal grouping
10	mdY	I – digital input	Signal configuring vertical foveal grouping
11	gndd	power	Ground connection
12	vddd	power	Power Supply for digital blocks
13	test_buffers	I – analog in	Analog input to test the analog output buffers
14	POE1	O –analog out	Ouput of the first analog test buffer
15	vddpwr	power	Power Supply for analog output buffers
16	Vgnbuff	I – analog in	Voltage bias of analog test buffers. Nom value=0.5V
17	POE2	O –analog out	Ouput of the second analog test buffer
18	bulk	power	Ground connection
19	qtest	O – digital out	Output of configuration shift register
20	Itest_ampN	O- analog out	Output current of N type current mirror-test of Ipots
21	Itest_ampP	O- analog out	Output current of P type current mirror-test of Ipots
22	gnd01_test	I – analog in	Analog voltage to set gain in test of low Ipot currents
23	vdd01_test	I – analog in	Analog voltage to set gain in test of low Ipot currents
24	gnd_ipots	power	Ground connection
25	Itest	O- analog out	Output current test of Ipots – both signs
26	Iref	I – analog in	Input current – usable as reference biasing current
27	vdd_ipots	power	Power Supply for ipots
28	in_reg	I – digital input	Input of the configuration shift register
29	clock	I – digital input	Clock of the configuration shift register
30	copy	I – digital input	Latch of the configuration shift register
31	reset_ipots	I – digital input	Reset the configuration shift register to default values
32	VGPAout	I/O-analog out	Output voltage of global adaptation/Voltage test input
33	NC	NC	Non Connected

34	NC	NC	Non Connected
35	NC	NC	Non Connected
36	VGPAsw	I-digital in	Control of switch connecting VGPAout
37	gnd_ana	power	Ground connection
38	vdd_ana	power	Analog power supply
39	Vrefoff	I – analog in	Voltage off threshold of pixel
40	Iave	0 –analog out	Current output of N-type measuring illumination level
41	bulk	power	Ground connection
42	Vpu3	I – analog in	Distributed-gate pull-up voltage. Optional.Default=gnd
43	Vpdx	I – analog in	Distributed-gate pull-down voltage. Opt.Default=vdd
44	Vpu	I – analog in	Distributed gate pull-up voltage. Optional.Default=gnd
45	Ack	I-digital in	Acknowledge for output address event
46	y<6>	O-digital out	Bit of Y-word of output address event
47	y<5>	O-digital out	Bit of Y-word of output address event
48	y<4>	O-digital out	Bit of Y-word of output address event
49	y<3>	O-digital out	Bit of Y-word of output address event
50	y<2>	O-digital out	Bit of Y-word of output address event
51	y<1>	O-digital out	Bit of Y-word of output address event
52	y<0>	O-digital out	Bit of Y-word of output address event
53	vddd	power	Power Supply for digital blocks
54	gndd	Power	Ground connection
55	Rqst	0-digital out	Request for output address event
56	x<7>	O-digital out	Bit of X-word of output address event
57	x<6>	O-digital out	Bit of X-word of output address event
58	x<5>	O-digital out	Bit of X-word of output address event
59	x<4>	O-digital out	Bit of X-word of output address event
60	x<3>	O-digital out	Bit of X-word of output address event
61	x<2>	O-digital out	Bit of X-word of output address event
62	x<1>	O-digital out	Bit of X-word of output address event
63	x<0>	O-digital out	Bit of X-word of output address event
64	reset	I-digital input	Reset of address event peripheral latches
65	gndd	Power	Ground connection
66	vddd	power	Power Supply for digital blocks
67	Vpu2	I – analog in	Distributed-gate pull-up voltage. Optional.Default=gnd
68	Vrefon	I – analog in	Voltage on threshold of pixel
69	Vref	I – analog in	Voltage reference threshold of pixel
70	VGPH	I – analog in	Voltage bias. Nominal value = 2.7V
71	VGPA	I – analog in	Voltage bias. Nominal value = 2.7V
72	vcas	I – analog in	Voltage bias. Nominal value = 1.65V
73	bulk	power	Ground connection
74	vdd_ana	power	Analog power supply
75	gnd_ana	power	Ground connection
76	fay<0>	I – digital input	Bit of y-word input address for foveal configuration
77	fay<1>	I – digital input	Bit of y-word input address for foveal configuration
78	fay<2>	I – digital input	Bit of y-word input address for foveal configuration
79	fay<3>	I – digital input	Bit of y-word input address for foveal configuration

80	fay<4>	I – digital input	Bit of y-word input address for foveal configuration
81	fay<5>	I – digital input	Bit of y-word input address for foveal configuration
82	fay<6>	I – digital input	Bit of y-word input address for foveal configuration
83	AEY	I – digital input	Enable all row selection for foveal config when high
84	AD	I – digital input	Disable signal of vert&horiz decoders for foveal config

Table 1. Pinout description of EF-DVS JLCC84 package

2.1 Sensor Foveal Control

Figure 3. illustrates the sensor architecture. Each pixel in the sensor receives two digital control signals m_{dY} and m_{dX} which are digitally stored and are individually reconfigurable for every pixel in the array.

When both signals m_{dY} and m_{dX} are simultaneously low, the pixel is operating individually in full HR mode. When signal m_{dY} the pixel is in low resolution and connected to its upper neighbor. Similarly, when m_{dX} is active the pixel is in low resolution and connected to its right neighbor. Using this scheme, low resolution regions with arbitrary shapes and sizes can be externally programmed in the sensor.

As shown in **Figure 3.** (a) the sensor contains an array of NxN pixels and the corresponding peripheral circuitry to generate the address-event-output. Additional X-FOV and Y-FOV foveation control blocks are added to the sensor for digital configuration of the foveal regions. **Figure 3.** (b) shows the schematic of X-FOV foveation block.

The sensor receives as input the address [***fax, fay***] of the pixel that should be reconfigured and the two bit digital configuration mode signal [m_{dX},m_{dY}]. The X-FOV and Y-FOV foveation control blocks contain decoders that activate the corresponding column and row signals [FX_i, FY_j]. The corresponding selected pixel where the [FX_i, FY_j] signals are simultaneously selected, updates it foveation configuration signals m_{dX} and m_{dY}. Additional control signals *AEX*, *AEY* and *AD* are added to the X-FOV and Y-FOV foveation control blocks to allow simultaneous configuration of all the array, all pixels in a row, or all the pixels in a column. Table 2 contains the output values of the X/Y-control foveation blocks as a function of the *AEX*, *AEY* and *AD* input values.

During single pixel configuration signals *AEX*, *AEY* and *AD* should be set to logic 1. Setting *AEX* to 0, all the column wise selection signals FX_i are simultaneously active, so that all pixels in the selected FY_j row are parallely configured with the same [m_{dX},m_{dY}] resolution configuration state. In a similar way setting *AEY* to zero, all row wise selection signals FY_j are simultaneously active, so that all pixels in the selected FX_i column are parallely configured with the same [m_{dX},m_{dY}] state. Setting *AEX* and *AEY* simultaneously to 0, allows parallel configuration of all the array pixels to the same [m_{dX},m_{dY}] state. Setting signal *AD* to 0 deactivates all row and column selection [FX_i, FY_j] signals disabling foveal reconfiguration.

AD / AE	0	1
0	1	0
1	1	FXj

Table 2. Logic output of the X/Y-control foveation blocks

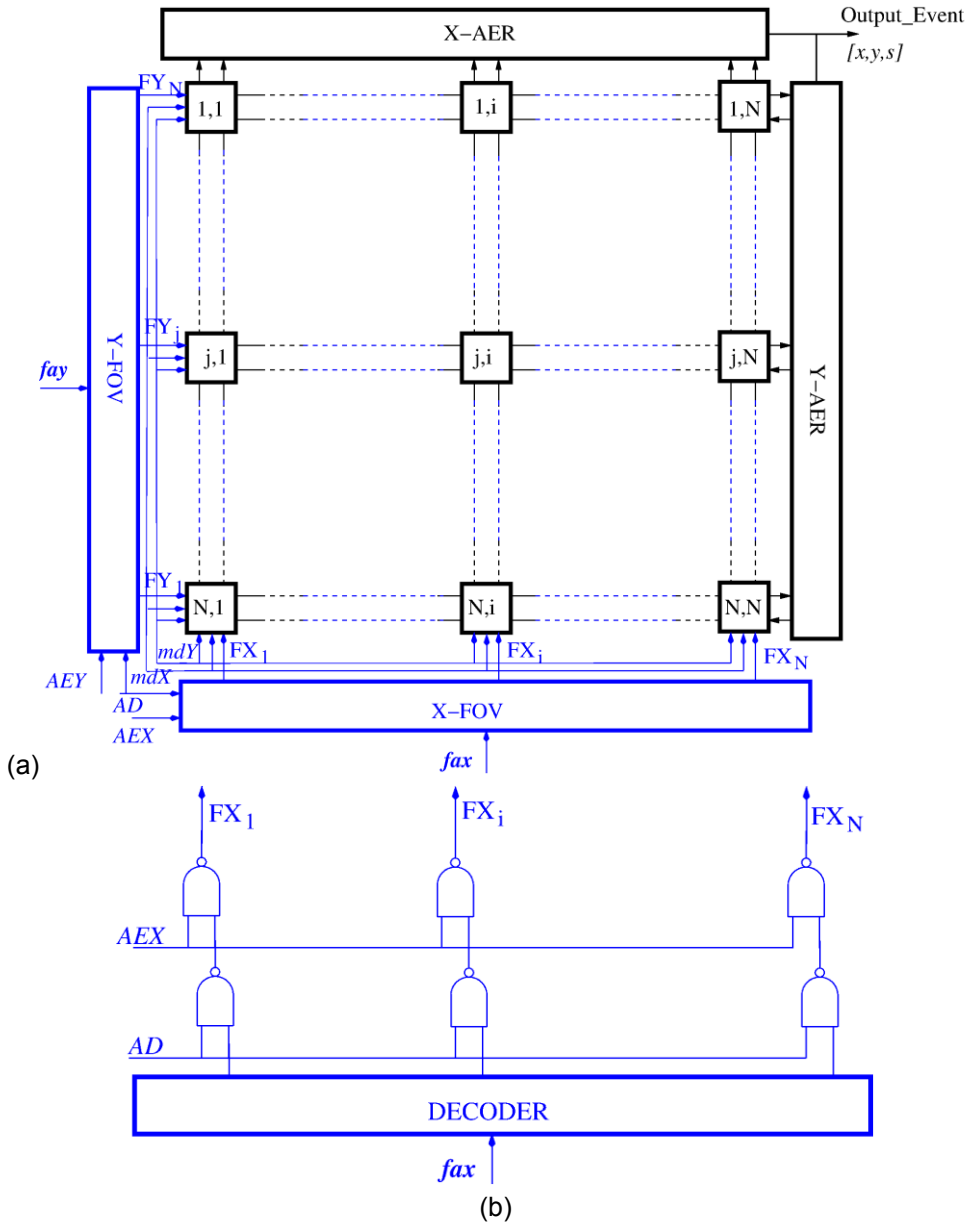


Figure 3. EF-DVS architecture. (a) Foveated DVS Array Architecture, (b) X-Foveation control

2.2 Sensor Voltage Biases

The sensor contains 13 voltage biases that are connected to 13 analog input pads. The table below contains the name given to the bias voltage pin and the number of the pin in the JLCC84 package as well as the default voltage value that should be used according to the design.
The voltage differences V_{ref}-V_{refoff} and V_{refon}-V_{ref} controls the sensor sensitivity to negative and positive changes in the illumination, respectively.
The voltage difference V_{GPH}-V_{GPA} controls a photocurrent amplification stage inside each pixel. This amplification can be used to adapt the sensor to global variations in the illumination condition.

The 13 voltage bias pins are connected in the test PCB to 4 chips of DACs, each one containing 4 DACs. These DACs are configured through a serial I2C bus using an STM32 microcontroller.

Bias Name	Retina Pin	DAC No	Description	Default Value
Vgnbuff	16	DAC<6>		0.4V
Gnd01_test	22	DAC<11>		0.1V
Vdd01_test	23	DAC<5>		3.2V
Vrefoff	39	DAC<10>		0.3V
Vpu3	42	DAC<14>		0V
Vpdx	43	DAC<13>		3.3V
Vpu	44	DAC<12>		0V
Vpu2	67	DAC<15>		0V
Vrefon	68	DAC<4>		0.55V
Vref	69	DAC<3>		0.45V
VGPH	70	DAC<2>		2.6V
VGPA	71	DAC<1>		2.5V
vcas	72	DAC<0>		1.65V

Table 3. Configuration of chip biasing voltages

2.3 Sensor Current Biases and Configuration of digital switches

Besides the voltage biases, the sensor uses 5 current biases and digital configuration bits that are programmed using and on-chip shift register and some on-chip programmable current biases named *I-pot* blocks [17]. Figure 8 illustrates the schematic of the current biasing and digital configuration blocks. The *Ipots_refFov* block generates the 5 biasing currents I_{bb}, I_{ab1}, I_{b1}, I_{brf} and I_{bo} that are programmed from a reference input current. A selection circuitry controlled by signal *sel_Iref* allows commuting the input reference current for *Ipot* block between an on-chip generated current (generated by a specific current extractor block[18] *is_extcasc*) and an externally provided current through pad I_{ref}. *Ipot* block and additional digital selection signals are configured using a shift register with digital input signals *in, clock, Copy*. *Ipot* circuits are externally measured and calibrated. For this purpose, each *Ipot* circuit output current can be selected and measured for each configuration word using an external output *Itest*. To be able to measure off-chip very low currents additional controllable amplifying current mirrors (MP5-MP8 and MN5-MN6) have been added that can be also selected using signal *sel_test_ampC*.

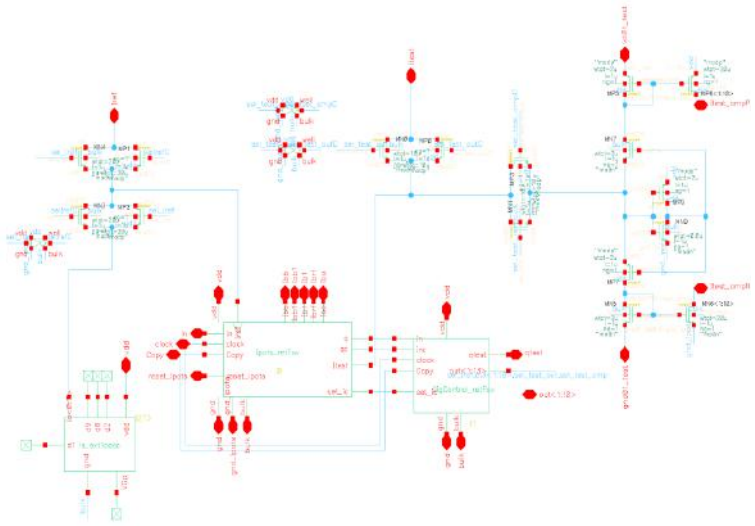


Figure 4. Schematic of the current biasing and digital configuration blocks

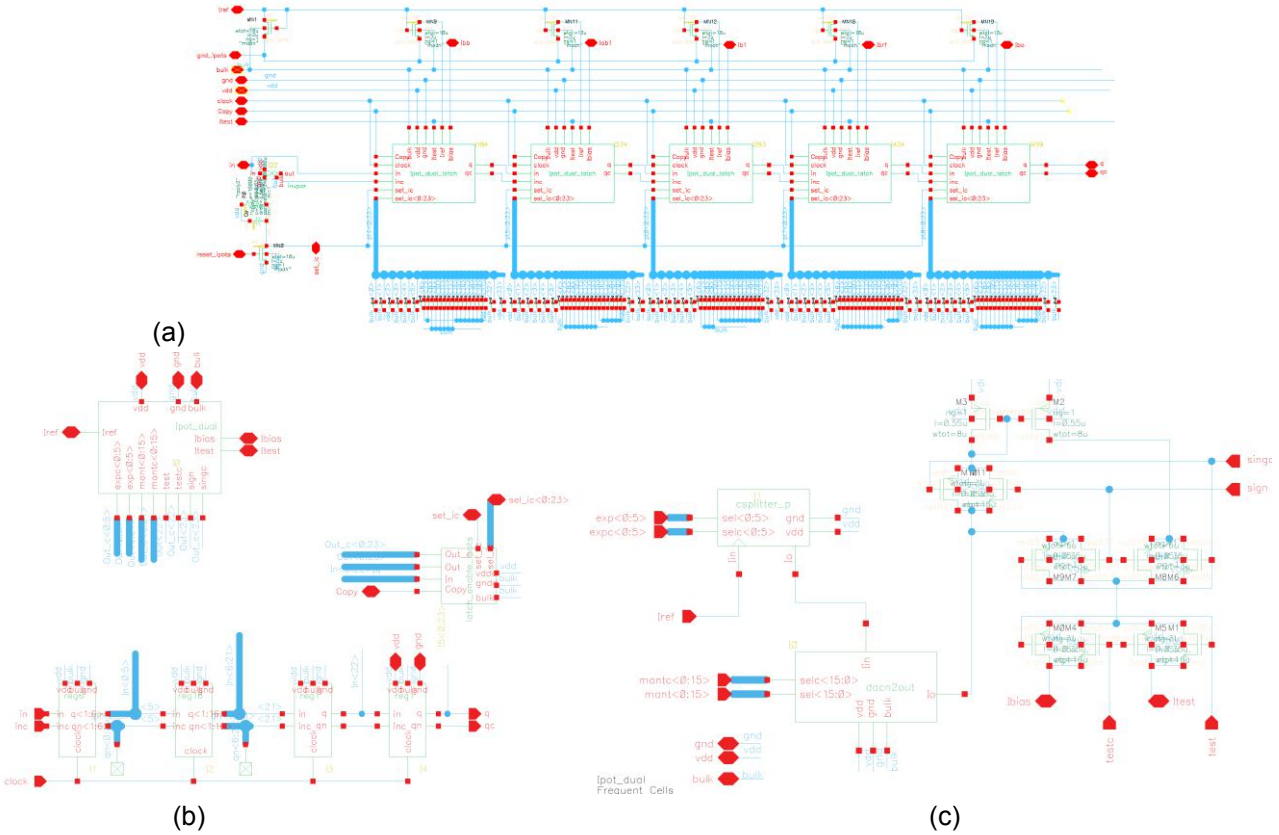


Figure 5. **(a) Schematic of Ipots chain for current biases control, (b) schematic of an Ipot including the digital shift register and the programmable current splitting ladders and (c) schematic of the programmable current splitting ladders**

Figure 5 details the schematic of the *Ipot* block. It contains five *Ipot* circuits[17]; one per bias current. Each *Ipot* circuit receives a copy of the input reference current and generates a bias current which is controlled by 24 configuration bits. The configuration bits are fed by a concatenated shift register and stored in latches as detailed in **Figure 5** (b). Each Ipot (see **Figure 5** (c)) contains two concatenated current splitters[19]. The first current splitter divides the input reference current *Iref*

in decades and is controlled by *exp<0:5>*, a 6 bit digital control word which selects the current range. In this exp<0:5> word, only one bit is simultaneously active. The second current splitter contains 16 branches with a fine grained current division factor. *Mant<0:16>* is a 16 bit control word with a combination of the 16 output branches for fine tuning the bias current value. Another *Ipot* controlling bit selects the current sign and a final test bit selects between the normal biasing output or the test output for externally characterizing the *Ipot* current. Table 4 contains the meaning of the 24 bit configuration word of each *Ipot* circuit.

As can be observed in **Figure 4**, the output of the *Ipot* block shift register is concatenated with an additional digital control block that stores 13 configuration bits. The total bit-length of the chip configuration shift register is 5X24+13= 133 bits. The role of the different configuration bits is detailed in Table 5. Signals *Bit<121:130>* are used to control the internal nodes that should be connected to the input of the test analogue buffers. Their default values for normal operation mode are listed in Table 5.

Register order	Bit<0:5>	Bit<6:21>	Bit<22>	Bit<23>
Ipot control	Exp<0:5>	Mant<0:16>	test	sign
	1-hot code	Fine-tuned code	0- bias current 1- test current	0–N-type current 1- P-type current

Table 4. Single Ipot configuration

Register Bit	Signal Name	Description	Ipot Type	Default Value
Bit<0:23>	Ibb	Bias Current of Pixel Buffer Stage	P-type (1)	001000 1100000011111111 0 1
Bit<24:47>	Iab1	Bias Current for Peripheral Adaptative Control	N-type (0)	100000 0000000001111111 0 0
Bit<48:71>	Ib1	Bias Current for Adaptative Control of Pre-amplifiers current gain	P-type (1)	001000 0000111111111111 0 1
Bit<72:95>	Ibrf	Bias Current for Refractory Period Control	N-type (0)	100000 0000000000011111 0 0
Bit<96:119>	Ibo	Bias Current of Photoreceptor source-driven active mirror	N-type (0)	100000 0000000001111111 0 0
Bit<120>	Sel_Iref	‘1’- Iref external; ‘0’ –on-chip current reference	N.A.	0
Bit<121>	En_buffer1	‘1’- Decoder buffer1; ‘0’- Disable decoder buffer1	N.A.	0
Bit<122>	Sel_buffer1<3>	Selection bit decoder buffer 1	N.A.	0
Bit<123>	Sel_buffer1<2>	Selection bit decoder buffer 1	N.A.	0
Bit<124>	Sel_buffer1<1>	Selection bit decoder buffer 1	N.A.	0
Bit<125>	Sel_buffer1<0>	Selection bit decoder buffer 1	N.A.	0
Bit<126>	En_buffer2	‘1’- Decoder buffer2; ‘0’- Disable decoder buffer2	N.A.	0
Bit<127>	Sel_buffer2<3>	Selection bit decoder buffer	N.A.	0

		2		
Bit<128>	Sel_buffer2<2>	Selection bit decoder buffer 2	N.A.	0
Bit<129>	Sel_buffer2<1>	Selection bit decoder buffer 2	N.A.	0
Bit<130>	Sel_buffer2<0>	Selection bit decoder buffer 2	N.A.	0
Bit<131>	Sel_test_out	'1'- Itest out connected to internal node, '0'-Itest out disconnected	N.A.	1
Bit<132>	Sel_test_amp	'1'-Ipots out connected to Itest_ampN/P, '0'-disconnected Itest_ampN/P	N.A.	0

Table 5. Configuration role of shift-register bits

The shift register is accessed through pins: 'in_reg', 'clock', 'copy', 'reset_ipots' and 'qtest'. Their operation and their pin out connection are described in Table 6

Each shift register cell stores a stable copy of the contents of its stored bit. The latches are controlled by a 'Copy' signal. When signal 'Copy' is '1' the signals from the shift register are copied into the latches (latches are transparent), when signal 'Copy' is '0' the contents of the latches are stored (latches are opaque). Latches can also be configured to some pre-defined hardwired default value by activating a signal 'Reset_ipots'. When 'Reset_ipots' is pulsed to '1', all the bits of the ipots are set to its default value described in the last column of Table 5. 'Reset_ipots' signal should be set to '0' during normal operation.

Pin Name	Retina Pin	Description
In_reg	28	Shift register input bit
Clock	29	Shift register clock signal. The shifting operates on the rising edge of the clock signal
Copy	30	Latch control. 'Copy' should be set to 1 to transfer the contents of the shift register and set to '0' afterwards.
Reset_ipots	31	Signal that allows to set the input to a default hardwired state. Signal should be to '1' to reset ipots configuration values and kept to '0' during normal operation.
qtest	19	Output pin of shift register. Only useful for test purposes.

Table 6. Description of Ipot pins

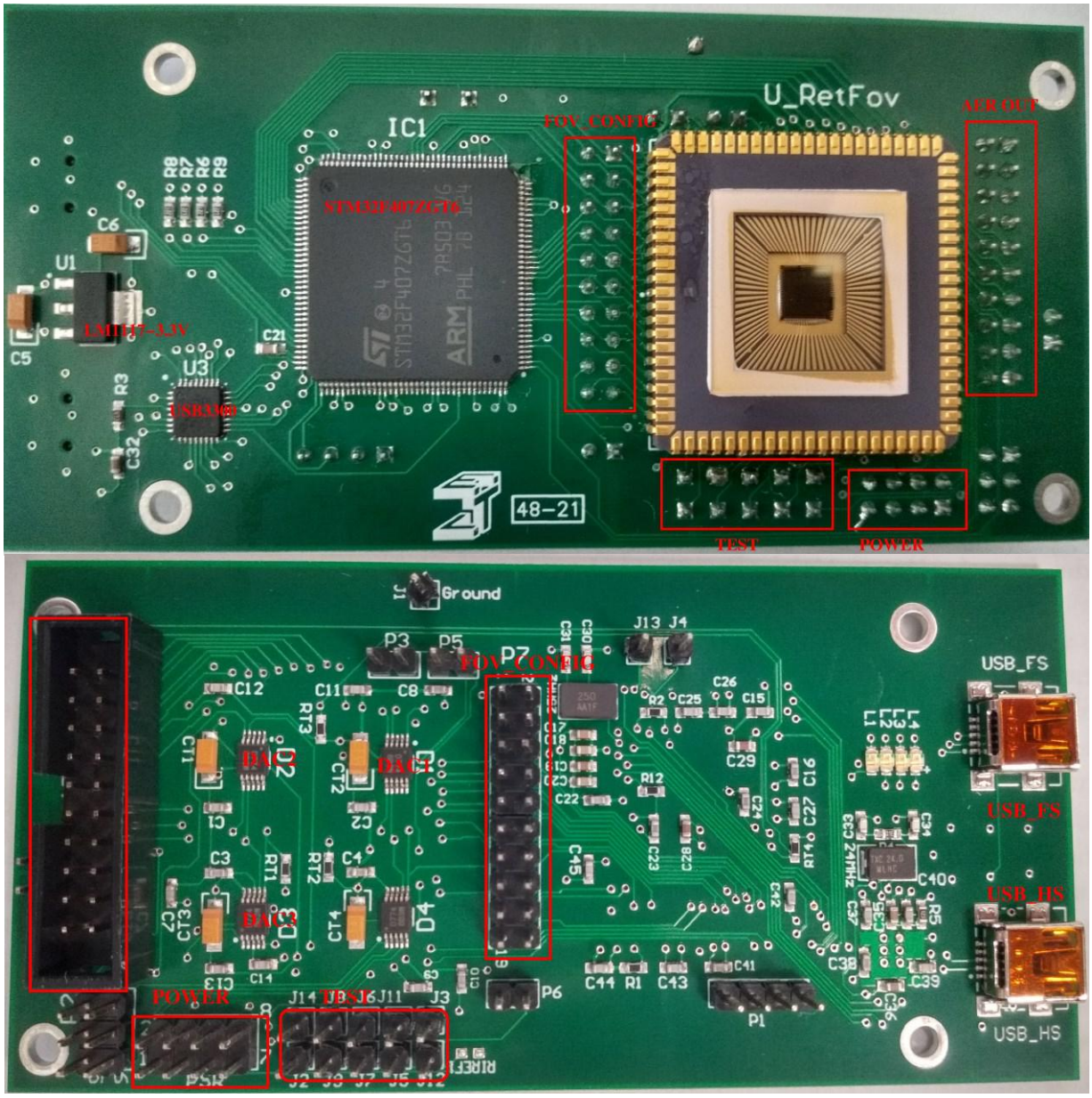


Figure 6. Schematic of PCB designed for the EF-DVS sensor

3 Test PCB Design

A PCB has been designed to test the EF-DVS sensor as shown in Figure 6. The PCB contains a STM microcontroller, the EF-DVS, some DACs, two USB connectors for microcontroller programming and communication, a parallel AER OUT output connector, a FOV_CONFIG parallel connector, as well as small connectors for signal output and signal testing.

Figure 8 contains a schematic representation of the two main AER_OUT and FOV_CONFIG connectors, where "R" means the connector pins are connected to output pins of the Retina and "M" means the connector pins are connected to the output pins of the microcontroller.

A high-level schematic representation of the interconnection between the STM microcontroller and the EF-DVS sensor is shown in Figure 7, where "C" means to connect to an output connector pin and "M" means to connect to the microcontroller input pin.

The microcontroller serves to communicate to a host computer through a USB connector and:

1. The value of the programmable biasing currents of the retina can be changed through the microcontroller, if needed.
2. Bias voltages are also set through the STMicrocontroller. There are four DAC chips (each one containing 4 individual DACs) on the PCB which are configured through I2C protocol that set the EF-DVS sensor voltage biases.
3. Digital outputs of the microcontroller connect to digital foveation control inputs in the EF-DVS. The operating mode of the retina (low or high resolution), as well as the region of interest, can be determined by the fay<0:6>, fax<0:6>, AEY, AD, AEX, mdX, and mdY digital signals which are generated by the microcontroller. These signals are also connected to the FOV_CONFIG connector for having external access, in that case, the corresponding output pins of the microcontroller should be set to high-impedance mode and the foveal configuration of the sensor can be programmed through the parallel FOV_CONFIG connector using an external alternative hardware.
4. AER<0:15> is the digital output word of the retina which represents the address event. This address is connected to the AER_OUT connector to have direct and external access and it is also connected to inputs of the microcontroller to have the possibility of using the output address events generated by the sensor for some real-time decisions on foveal configuration using the microcontroller.

MATLAB functions and a graphical user interface (GUI) have been developed that allows the voltage, current biasing, and control of the sensor operation through a host external PC using the microcontroller as interface.

fay<0:6>	I – digital input	Bits of input address for foveal configuration
AEY	I – digital input	Enable all row selection for foveal config when high
AD	I – digital input	Disable signal of vert&horiz decoders for foveal config
fax<0:6>	I – digital input	Bits of address for foveal configuration
AEX	I – digital input	Enable all column selection in foveal config when high
mdX	I – digital input	Signal configuring horizontal foveal grouping
mdY	I – digital input	Signal configuring vertical foveal grouping
AER<0:6>	O-digital out	Bits x<6:0> output event address
AER<7>	O-digital out	Event sign
AER<8:14>	O-digital out	Bits y<0:7> output event address

Table 7. Correspondence between sensor input/output signals and connectors AER_OUT, FOV_CONFIG

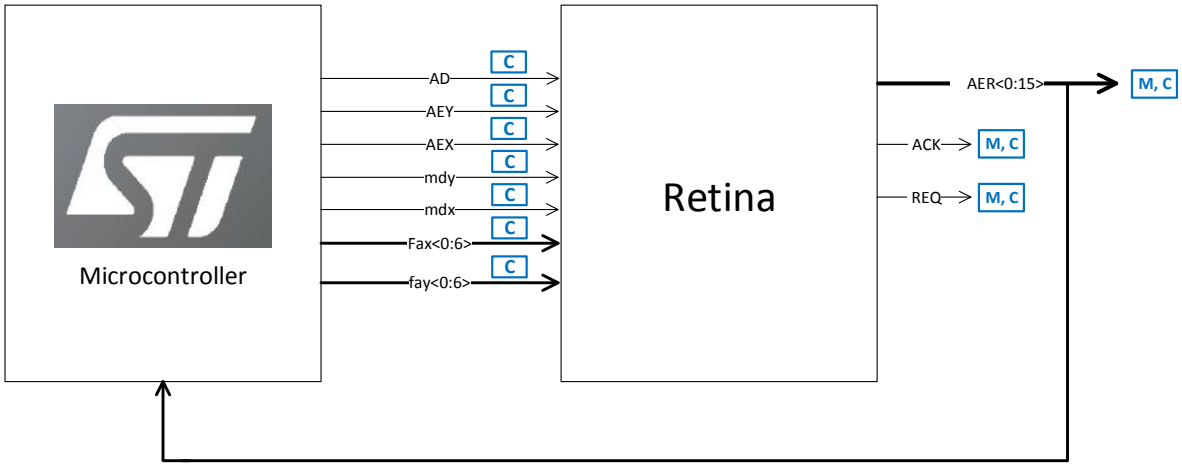


Figure 7 Board-Level diagram of the Retina and microcontroller connection

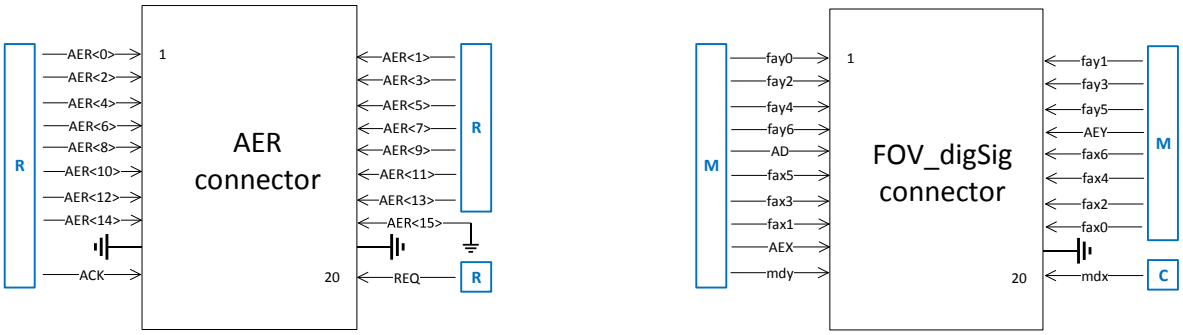


Figure 8 Board-Level diagram of the main connectors. (Left) DVS event output AER OUT connector. (Right) FOV CONFIG Connector for digital input signals to control the region of interest.

3.1 Configuration of current biases and digital switches

As described in subsection 2.3, the retina has 5 current biases and 13 digital switches that enable selection and external observation of some internal analog nodes. The current biases and digital switches are configured through a shift register. Previous to the use of the sensor, the ipots are characterized and the measured currents as a function of the digital configuration are stored. During the normal sensor use, this stored table is used to set the optimum digital configuration that produces the closest current to the target one set by the user. Once the optimum configuration for the 5 current biases and the state of the 13 digital switches are set by the user, the microcontroller feeds the corresponding configuration to the chip shift register. The target current values and the state of the 13 digital switches are entered by the user using the matlab GUI shown in Figure 9(a).

3.2 Sensor Voltage Biasing

As described in subsection 2.2 and detailed in Table 3, the configuration of 13 voltage biases is also required for the sensor operation. In the test PCB, these 13 voltage biasing output pins in the sensor are connected to DAC chips that are configured with the STMicrocontroller through I2C buses. The user sets the values of the target voltage biases through the Matlab GUI as shown in Figure 9(b).

3.3 Sensor Resolution Configuration

For controlling the sensor resolution several functions has been implemented in the STMicrocontroller that generate the control signal to configure the EF-DVS in the desired resolution. A matlab GUI shown in Figure 9(c) calls the resolution configuration functions and sends the corresponding parameters. As can be seen in Figure 9(c) the sensor can be put in high-resolution, all the pixel array can be configured in low resolution regions of size WxL, high resolution foveal regions with center (x_0,y_0) and size l_0xw_0 can be configured, or a low resolution region of size l_0xw_0 centered at (x_0,y_0) with patches of WxL can be configured.

3.4 Sensor Events Read Out

The read out of the sensor can be done using the matlab GUI interface shown in Figure 9(d) that uses the STmicrocontroller to do the handshaking with the Ack/Rsqt signals of the EF-DVS and receives the addresses of the output events adding a timestamp. The timestamped events are sent to a host PC through the USB interface and stored in a text file.
However, the addresses and handshaking signals are also connected to the parallel AER OUT connector. This connector is usually used to connect a neuromorphic processor for real-time processing of the events or to an FPGA-based board such as the USB-miniAER2[20] for high-speed timestamping and USB sending of the output events.

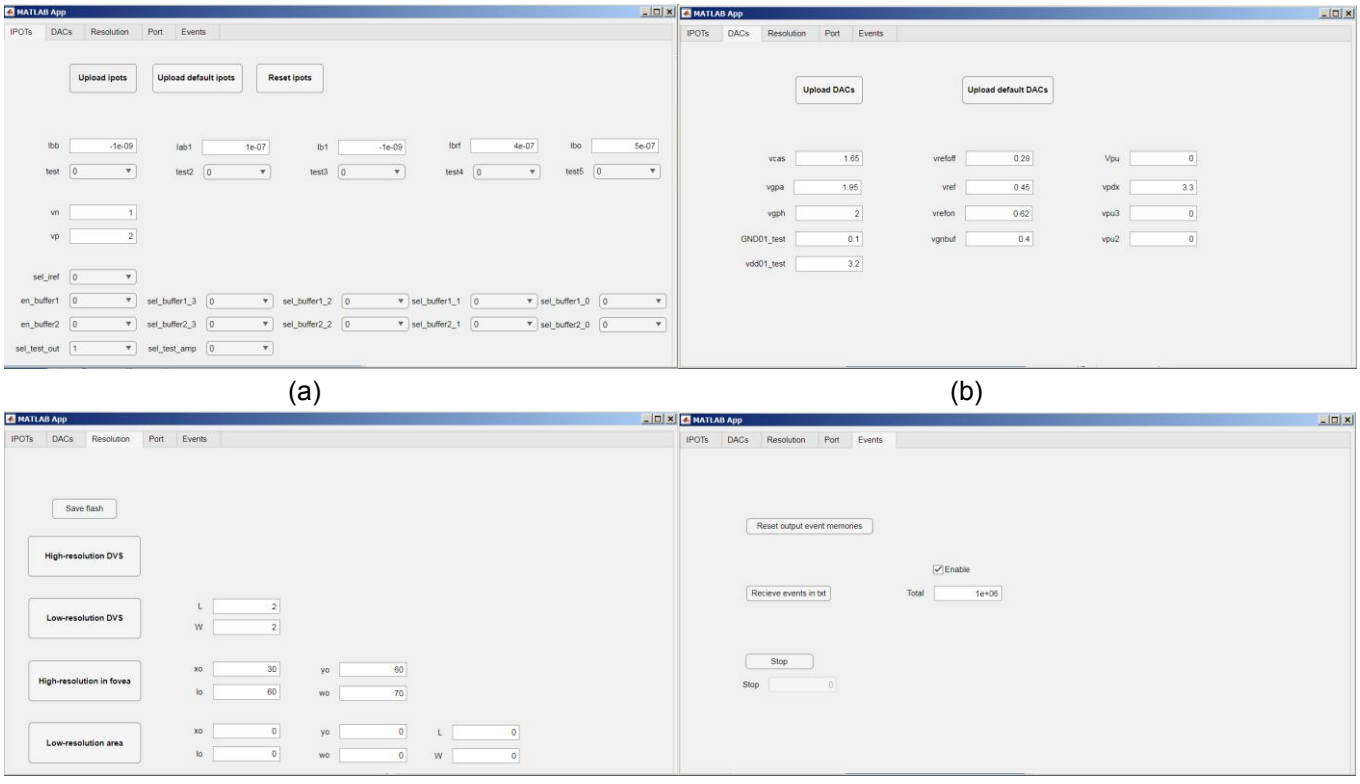


Figure 9. Matlab GUI for the sensor configuration. (a) Tab for Ipots configuration, (b) tab for voltage biases configuration, (c) tab for sensor resolution configuration, and (d) tab for capturing output events using the STM32 microcontroller.

3.5 Configuration of other external control signals

The chip has only one additional digital input signal V_{GPAsw} that should be configured externally. V_{GPAsw} controls a switch that connects/disconnects pad V_{GPAout} to the internal node $V_{GPAperi}$. During normal operation this signal should be set to '0'.

4 Preliminary Experimental Results

The EF-DVS has been mounted in an optical test bench for experimental characterization. Figure 10 shows a photograph of an experimental set-up where the sensor is illuminated with a background illumination generated by a fluorescence lamp and a diode driven by a sinusoidal signal is used to test the sensor bandwidth. Additional, neutral density filters can be used to characterize the sensor behavior under different illuminations.

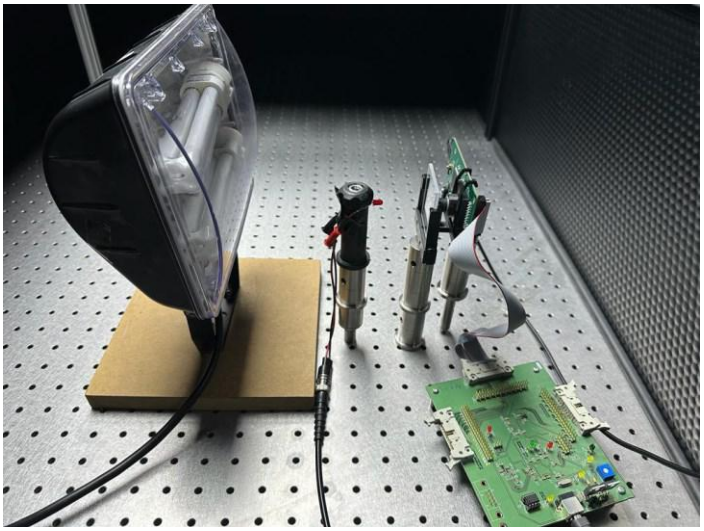
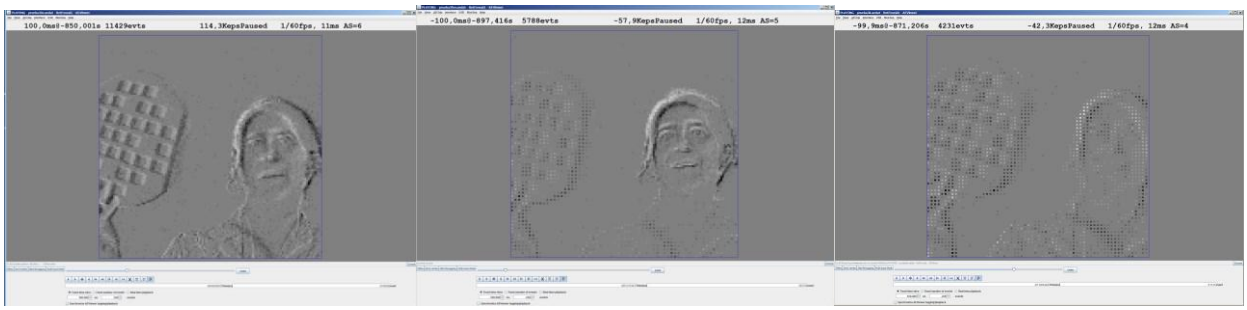


Figure 10. Experimental set-up for EF-DVS characterization in the laboratory optical test bench.

4.1 Test of foveal behaviour and resolution control

As preliminary test, the correct operation of the EF-DVS electronic control of the sensor resolution and configuration of foveal regions has been checked. Figure 11 shows the results of histogramming the sensor output events during 100ms when observing the same scene under 3 different sensor resolution configurations.



(a) (b) (c)

Figure 11. Event histogram of 100ms captured by the EF-DVS observing the same scene with different resolution configurations. (a) Full sensor in high resolution configuration, (b) Sensor in 2x2 resolution mode with a foveal high resolution region centered in the human face, and (c) Full sensor in 2x2 low resolution mode.

5 Future Work

After developing the test set-up and testing the correct functionality of the sensor programming and check the sensor basic functionality, the test of the sensor to deeply characterize bandwidth, latency, mismatch and current consumption in different sensor resolution configurations is currently being done.

A new EF-DVS sensor in an advanced XFAB 180nm technology has been designed and sent for fabrication. The new foveated pixel occupies a reduced area. A 2x2 array of dvs pixels in the xfab 0.18 um technology occupies 35.1 um x 35.85um. A proof of concept 64x64 EF-DVS sensor has been submitted for fabrication in XFAB 180nm. The test chip also contains isolated photoreceptors to test their optical efficiency and decide the size of the photoreceptor in a higher resolution final prototype.

6 Publications

1. T. Serrano-Gotarredona and B. Linares-Barranco, *patent - Electronically Foveated Dynamic Vision Sensor*, ES1641.1671, October 5th 2021, CSIC (90%) and Universidad de Sevilla (10%).
2. T. Serrano-Gotarredona, F. Faramarzi and B. Linares-Barranco, "Electronically Foveated Dynamic Vision Sensor," IEEE International Conference on Omni-Layer Intelligent Systems, Barcelona, August 1-4, 2022
3. T. Serrano Gotarredona and Bernabe Linares-Barranco " System Architectures for Electronically Foveated Dynamic Vision Sensor" , Conference on Design of Circuits and Integrated Systems - DCIS 2022, Pamplona, November 16-18, 2022

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8 Documentation

8.1 Applicable and Referenced Documents

#	Id	Description	Identifier (Ed Rev)	Date
AD1	FPP	Full Project Proposal	1.0	15.01.2019
D2.1.1		EF-DVS Sensor Design		

8.2 Glossary and Terminology

Acronym	Definition
AER	Address Event Representation
AMS	Austrian Micro Systems
DVS	Dynamic Vision Sensor
EF-DVS	Electronically Foveated Dynamic Vision Sensor
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HR	High Resolution
JLCC	J-Leaded Ceramic Carrier
LR	Low Resolution
ROI	Region of Interest
DAC	Digital Analogue Converter
USB	Universal Serial Bus
PCB	Printed Circuit Board
I2C	Inter Integrated Circuit